5 pts

TITLE

Low-voltage IC-circuit.

AREA OF THE INVENTION

The invention concerns a low-voltage IC-circuit construction.

BACKGROUND OF THE INVENTION

Starting with the 0.35μm generation, CMOS scaling has changed from a constant-voltage regime with a nominal supply voltage of 5V to a constant-field regime where the supply voltage is being reduced in concert with geometric dimensions with each process generation. We are thus likely to see more and more CMOS circuits in the future that must operate with a supply voltage below that of the usual sources of electrical energy. As an example, consider a 1.2V battery cell that feeds a low-power low-voltage circuit operating at a mere 0.6V. The most obvious solution is to use a voltage converter in down mode. While this is possible, the converter is costly, space consuming, and also has its own power dissipation. The object of the invention is to provide a low-voltage IC circuit that can be powered from a supply with a higher voltage than what is required by the IC, without having to use a down converter.

SUMMARY OF THE INVENTION

According to the invention, the circuit on the IC is partitioned into power consuming sub-circuits each of which is to be fed with its own supply voltage and the sub-circuits are then connected in series.

This effectively cuts the supply voltage for each sub-circuit. In this way it becomes possible to use a battery cell with a high voltage to feed a low voltage circuit without the need to provide the usual down converter.

Preferably a control circuit is provided in order to balance the voltage drops across the power consuming sub-circuits whereby constant voltage-drops over the sub-circuits are maintained. Even if great care is taken during design of the sub-circuits, it cannot be ensured that the current drain will always remain the same over the sub-circuits. The control circuit provides the means by which a uniform power supply to the sub-circuits can be maintained in such cases.

The sub-circuits may be digital or analog or mixed signal circuits. Also the number of series-connected sub-circuits is not limited.

The division into independent power consuming sub-circuits which are connected in series is feasible in both analog and digital blocks of an IC.

The IC circuit according to the invention may be partitioned such that the sub-circuits are located on each their chip.

This can be an advantage, when very large circuits are in use, or where other reasons are present for locating various parts of the circuit on different chips.

In a preferred embodiment two sub-circuits are series-connected such that the ground level (VHH) in the power supply of the first sub-circuit is used as supply level in the second sub-circuit.

The use of two sub-circuits makes the control circuit particularly simple to implement.

According to a further embodiment of the invention the control circuit comprises a first buffer capacitor coupled in parallel over the supply (VBB) and ground (VHH) level of the first sub-circuit and a second buffer capacitor coupled in parallel over the supply level (VHH) and the ground (GND) of the second sub-circuit, and whereby means for maintaining a uniform voltage drop over the first and the second buffer capacitor comprises at least one bucket capacitor which is alternately coupled in parallel over the first and the second buffer capacitor through a switching system controlled by a suitable signal that toggles at a sufficient rate.

The provision of the buffer capacitors will help to stabilize the voltage over the two sub-circuits, by absorbing fast transients in the current consumption. The alternately coupled buffer capacitor is a very simple and elegant way of maintaining a uniform voltage drop over the two buffer capacitors and, hence, also the two sub-circuits. Also this solution recycles excess energy and is thus an energy-efficient way of balancing the voltage drops across the two power consuming sub-circuits.

In an embodiment of the invention there are two bucket capacitors that get switched at the same time such as to alternately couple to the first and the second buffer capacitor respectively.

This solution is somewhat more complicated than the solution with only one bucket capacitor, but on the other hand it will assure an even smaller ripple in the supply voltages to the two sub-circuits.

Preferably the switches for alternately coupling the bucket capacitors are controlled by a free-running oscillator, a clock, or some other suitable signal that toggles at a sufficient rate to allow for a near-perfect voltage balance.

This is possible because of the self-regulatory function of the stabilizer circuit, and it is a great advantage, as it keeps the necessary circuit overhead down, and thus provides IC units which are cheaper.

In an embodiment of the invention, the means for maintaining a uniform voltage drop over the first and the second buffer capacitor comprises a voltage reference and a comparator, which generates control signals for voltage control means.

This is more complicated, but it is possible through this to maintain a very uniform voltage with little or no ripple.

In an embodiment of the invention, the midpoint stabilizer is designed such as to deliberately maintain different voltage drops across the sub-circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an overall circuit arrangement according to the invention,
Figs. 2- 5 are different embodiments of the midpoint stabilizers.

DESCRIPTION OF A PREFERRED EMBODIMENT

The overall circuit organization is shown in fig. 1. The two complementary subsets of the payload circuit are connected in series. The first sub-circuit 1 of the payload circuitry has a power supply line 2, which maintains the voltage level of VBB and a ground connection 3, which is to maintain voltage level VHH. The ground connection 3 is also routed to the midpoint stabilizer 4 and functions as power supply line to the further sub-circuit 6 of the payload circuitry. This sub-circuit 6 further has a ground connection 7 with the voltage level of GND. The midpoint stabilizer 4 ensures that the voltage in the power supply line 3 to the sub-circuit 6 remains constant and at the midpoint between the battery supply voltage VBB and the ground level GND. Level shifters 8 are mandatory wherever a signal crosses over from the lower partition to the upper partition or vice versa. Depending on the peripheral voltage levels, level-shifters 9 are likely to be required on input and output signals as well.

Balancing the voltage drops across the two sub-circuits 1,6 in fig. 1 of the payload circuit requires that they exhibit identical current drains and activity profiles. Of course, one will strive to obtain a good balance during the design process, yet matching the two sub-circuits statically does not suffice because supply currents inevitably vary over time. Buffer capacitors help to absorb brief current surges. The residual disparities are compensated for by a midpoint stabilizer circuit 4. Four alternative circuits are proposed according to figs. 2-5.

In the following, details of the mid-point stabilizers in figs 2-5 are explained. Any of these drawings fits into fig.1 as midpoint stabilizer circuit 4 and connects by way of

common circuit nodes including the three voltage levels VBB, VHH and GND through lines 2,3 and 7 respectively. All implementations share the goal of making the voltages across the two payload circuits 1 and 6 in fig.1 the same. What all stabilizers further have in common is the presence of two buffer capacitors 10 and 11 in figures 2-5 that store short-term energy and so reduce supply voltage ripple for the payload circuits.

Fig. 2 shows a first implementation of a midpoint stabilizer. Comparator 12 constantly evaluates the voltages across the two payload circuits against their intended values. If an asymmetry begins to develop, comparator 12 either closes switch 13 or14 in order to pump extra charge into circuit node 3 to raise the voltage level of VHH or to blow off excess charge from it through resistor 15 or 16 respectively until VBB-VHH and VHH-GND match. Switches 13 and 14 and/or resistors 15 and 16 may or may not be implemented as transistors (field-effect transistor FET or bipolar junction transistor BJT, switches in micromechanical technologies, or any other electrically controlled devices). Fig. 3 is much the same with the switches and resistors replaced by controlled current sources 17 and 18. Again, the controlled current sources may or may not be implemented as transistors (field-effect transistor FET or bipolar junction transistor BJT, switches in micromechanical technologies, or any other electrically controlled devices).

As opposed to this, the circuits of figs. 4 and 5 include no dissipative shunts in their circuits. Instead, they feature extra capacitors that act as buckets for charge transfer. Fig. 4 includes one such bucket capacitor 20 that gets rapidly switched back and forth between the upper and lower payload circuit as the two-throw switches 25 and 28 alternate between their two stable positions. The bucket capacitor 20 accepts extra charge at the higher of the two voltages (VBB-VHH and VHH-GND) and releases that charge at the lower voltage thereby compensating for any momentary difference in the current drains of the two payload circuits. Fig. 5 is more sophisticated in that it includes two such bucket capacitors 21 and 22 and four switches 35, 36, 37 and 38. The advantage is that one can obtain the same low supply voltage ripple with smaller buffer capacitors because one of the buckets picks up charge at the higher voltage while the other one releases charge at the lower level at any time. Again, switches 25 and 28 in fig. 4 and 35, 36, 37 and 38 in fig. 5 may or may not be implemented with the aid of transistors (field-

effect transistor FET or bipolar junction transistor BJT, switches in micromechanical technologies, or any other electrically controlled devices).

A point that deserves special attention is the fact that all switches in figs. 4 and 5 can be controlled by a free-running oscillator 27, a clock, or some other signal that toggles frequently enough. There is no need to sense and compare the supply voltages across the payload circuits as the rapid switching of the bucket capacitors will naturally tend to make them equal, provided there is no excessive disparity in the respective current consumptions of the two payload circuits.

Proposals in fig. 4 and 5 are particularly attractive because they do not make use of any dissipative shunts but recycle excess energy with the aid of capacitors that get switched from the lower partition to the upper one and back again. Also they function in a self-regulating way as there is no need to steer the switching of those charge buckets except, possibly, for avoiding unnecessary switching activity. Though inferior in terms of performance to fig. 5, fig. 4 would perhaps be a reasonable compromise between energy efficiency, supply ripple and circuit overhead (i.e. cost).

CLAIMS

1. IC-circuit construction whereby the circuit on the IC is partitioned into power consuming sub-circuits (1,6) which each has a power supply, and whereby the sub-circuits (1,6) are connected in series.

2. IC-circuit as claimed in claim 1 whereby a control-circuit (4) is provided in order to balance the voltage drops across the power consuming sub-circuits (1,6) whereby constant voltage-drops over the sub-circuits (1,6) are maintained.

3. IC-circuit as claimed in claim 1 or claim 2 whereby the sub-circuits (1,6) are digital or analog or mixed signal circuits.

4. IC circuit as claimed in claim 1 whereby the sub-circuits (1,6) are located on each their chip.

5. IC circuit as claimed in any of the above claims, whereby two sub-circuits (1,6) are series-connected such that the ground voltage level (VHH) in the power supply of the first sub-circuit (1) is used as the supply voltage level in the second sub-circuit (6).

6. IC circuit as claimed in claim 5, whereby the control circuit comprises a first buffer capacitor (10) coupled in parallel over the supply voltage level (VBB) and ground voltage level (VHH) of the first sub-circuit (1) and a second buffer capacitor (11) coupled in parallel over the supply voltage level (VHH) and the ground voltage level (GND) of the second sub-circuit (6), and whereby means for maintaining a uniform voltage drop over the first (10) and the second (11) buffer capacitor comprises at least one bucket capacitor (20,21,22) which is alternately coupled in parallel over the first (10) and the second (11) buffer

capacitor through a switching system controlled by a signal that toggles at a sufficient rate.

7. IC circuit as claimed in claim 6, whereby there are two bucket capacitors (21,22) that get switched at the same time such as to alternately couple to the first and the second buffer capacitor respectively.

8. IC circuit as claimed in claim 6 or 7, whereby the switches (25,28,35,36,37,38) for alternately coupling the bucket capacitors (20,21,22) are controlled by a free-running oscillator (17), a clock, or some other suitable signal of periodic or nonperodic nature.

9. IC circuit as claimed in claim 6, whereby the means for maintaining a uniform voltage drop over the first (10) and the second (11) buffer capacitor comprises a voltage reference and a comparator (12), which generates control signals for voltage control means.

10. IC circuit as claimed in claim 2 whereby the control circuit (4) is designed such as to maintain different voltage drops across the sub-circuits (1,6).

ABSTRACT

The invention regards an IC-circuit construction whereby the circuit on the IC is partitioned into power consuming sub-circuits which each has a power supply, and whereby the sub-circuits are connected in series. According to the invention various ways of assuring stable voltage drop over each sub-circuit are suggested.

Fig. 1

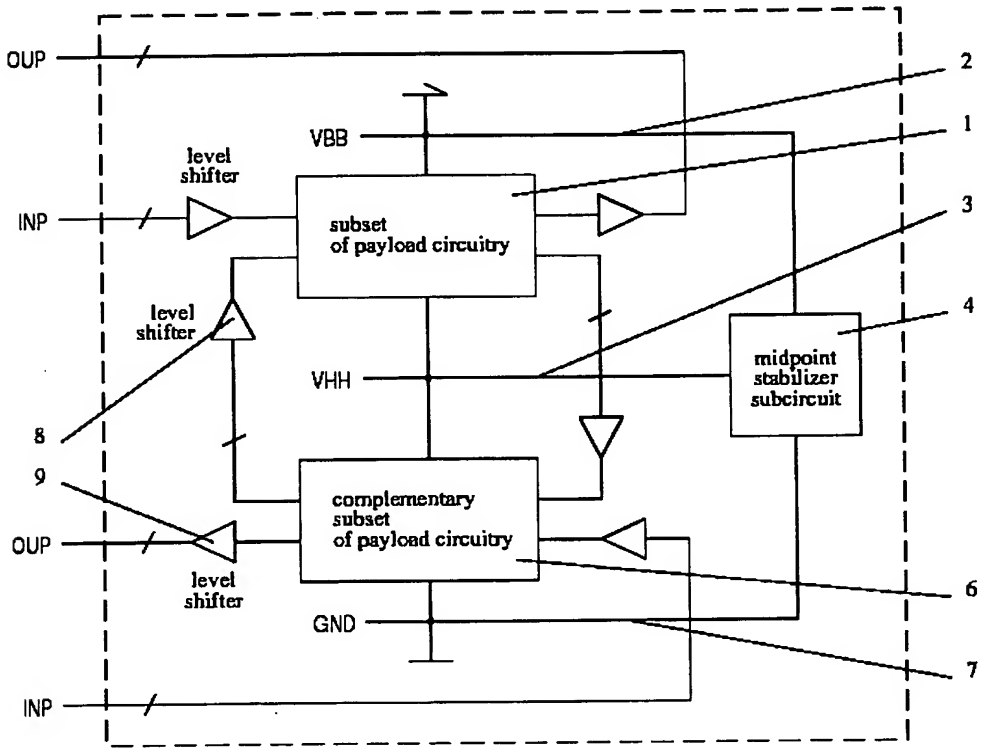
OUP
INP
level shifter
VBB
subset of payload circuitry
level shifter
VHH
midpoint stabilizer subcircuit
8
9
OUP
level shifter
complementary subset of payload circuitry
GND
INP
1
2
3
4
6
7

Fig. 1

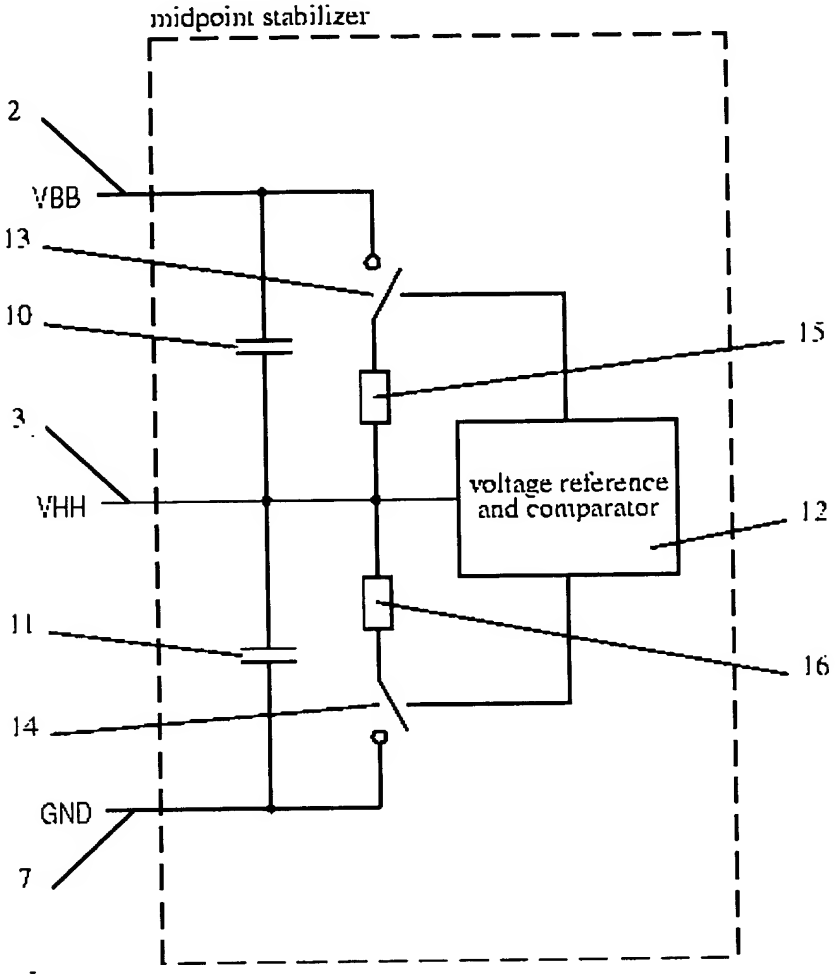
midpoint stabilizer
2
VBB
13
10
15
3
VHH
voltage reference and comparator
12
11
16
14
GND
7

Fig. 2

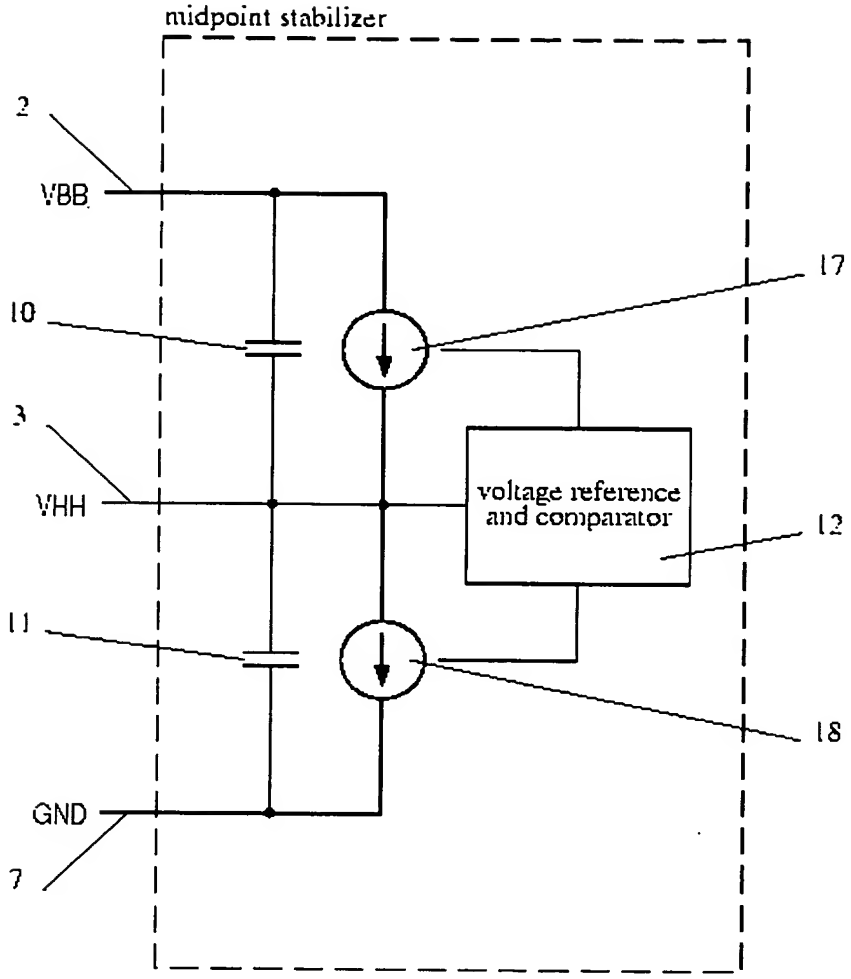
midpoint stabilizer
2
VBB
17
10
3
VHH
voltage reference and comparator
12
11
18
GND
7

Fig. 3

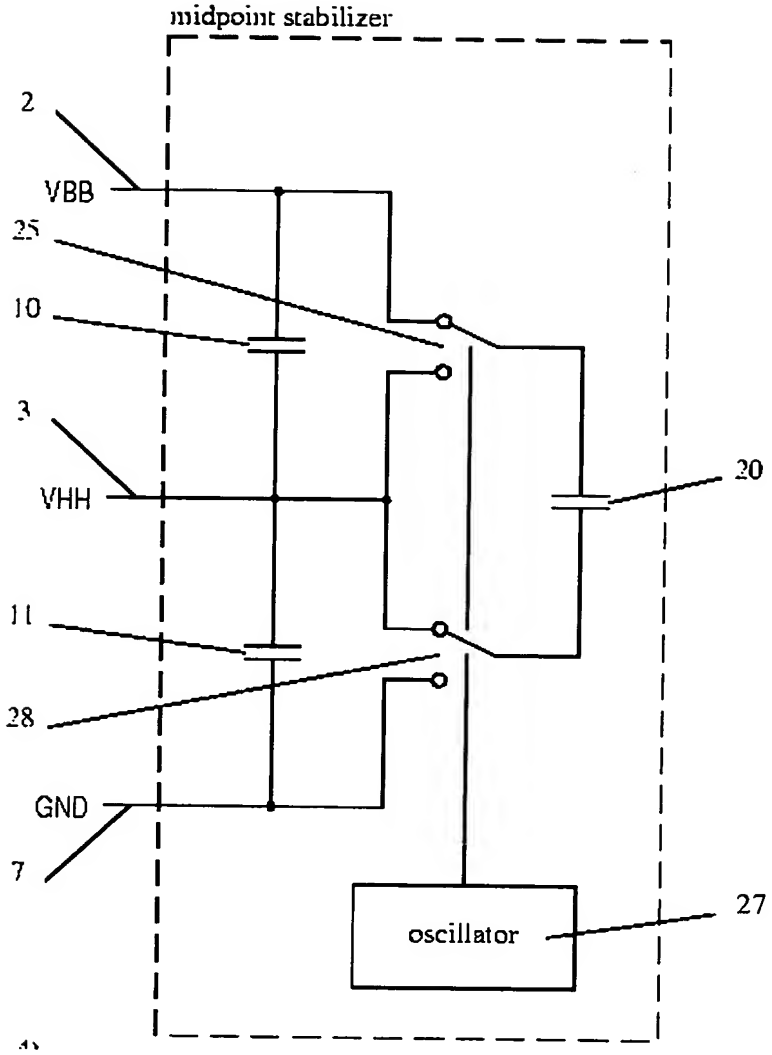
midpoint stabilizer
2
VBB
25
10
3
VHH
20
11
28
GND
7
oscillator
27

Fig. 4

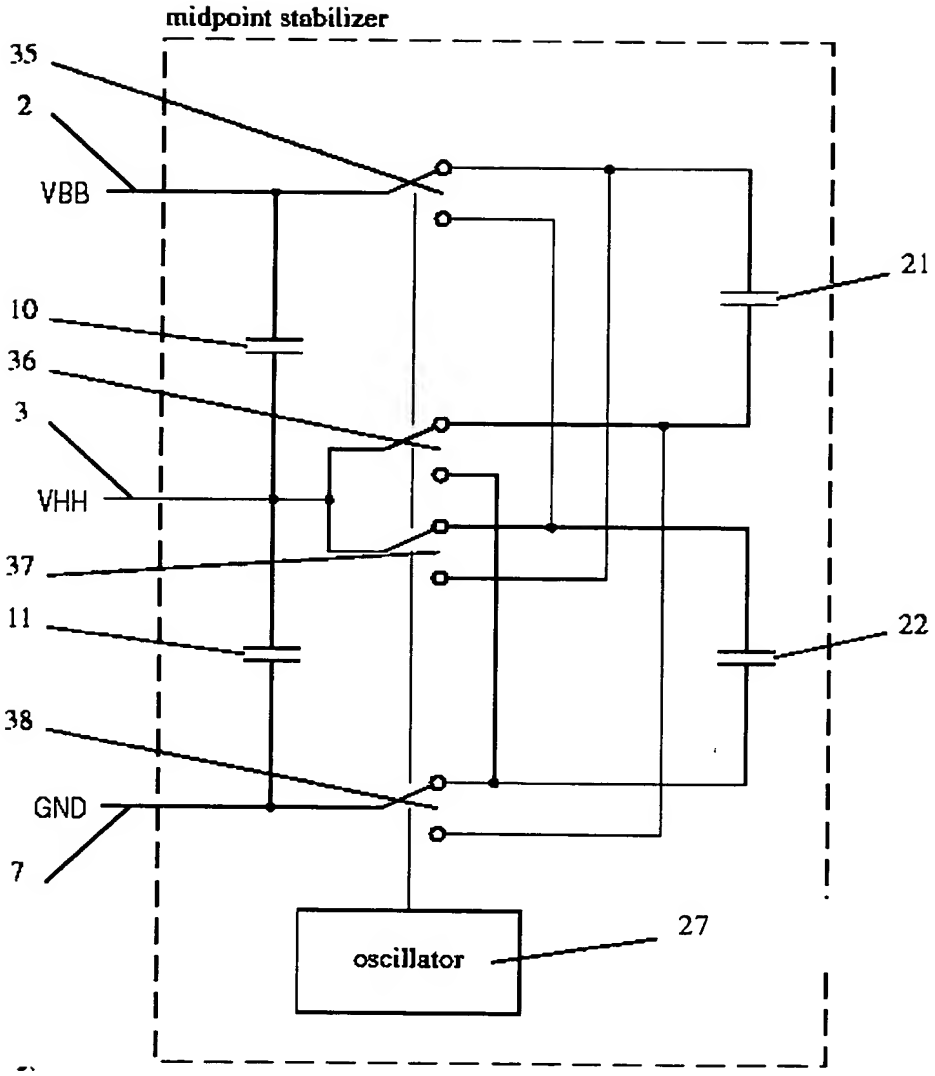
midpoint stabilizer
35
2
VBB
10
36
3
VHH
37
11
38
GND
7
21
22
27
oscillator

Fig. 5